KT SEMICON
Technology for Tomorrow

Job Title: Design & Verification engineer
Location: Hyderabad
Type: Full-time
Experience Level: 0 – 1 Year

Job Summary:
We are looking for a highly motivated and skilled VLSI Design & Verification (D&V) Engineer to join our growing engineering team. The ideal candidate will be responsible for verifying complex digital designs, ensuring their functional correctness, performance, and adherence to specifications. This role involves developing robust verification environments, executing comprehensive test plans, and debugging design issues to contribute to the successful tape-out of next-generation silicon.

Key Responsibilities:

- **Verification Plan Development:** Develop detailed functional verification plans based on design specifications and architecture documents.
- **Testbench Development:** Architect, design, and implement advanced verification environments (testbenches) using industry-standard methodologies such as UVM (Universal Verification Methodology) or other System Verilog-based approaches.
- **Test Case Development:** Write and debug highly effective directed and constrained-random test cases to achieve

comprehensive functional coverage and expose corner-case scenarios.

- **Simulation & Debugging:** Execute simulations, analyze waveforms, and perform root-cause analysis to identify and debug complex design and testbench issues.
- **Coverage Closure:** Drive functional coverage closure, including code coverage, functional coverage, and assertion coverage. Develop new tests or modify existing ones to fill coverage holes.
- **Assertions:** Implement assertions (SVA - System Verilog Assertions) to monitor design behavior and detect design bugs early.
- **Regression Management:** Manage and maintain regression suites, ensuring efficient execution and analysis of results.
- **Collaboration:** Work closely with RTL design engineers to understand design intent, review specifications, and debug design issues. Collaborate with architecture, software, and physical design teams as needed.
- **Flow & Methodology Improvement:** Contribute to the enhancement of existing verification flows, tools, and methodologies.
- **Documentation & Reporting:** Create and maintain clear, concise documentation for verification plans, environments, and test results. Provide regular status updates and reports.
    - **Performance Verification (Optional/Advanced):** Experience with performance verification, power verification, or formal verification is a plus.

Required Skills:

- Strong Digital Design Fundamentals: In-depth understanding of digital logic, computer architecture, microprocessors/microcontrollers, FSMs, and clock/reset methodologies.
- Hardware Description Languages (HDLs): Expert proficiency in Verilog and/or VHDL for RTL design understanding.
- Verification Methodologies: Strong expertise in System Verilog and UVM for building robust verification environments.
- Testbench Architecture: Solid understanding of advanced testbench architectures, including components like transactors, sequencers, drivers, monitors, and scoreboards.
- Functional Coverage: Experience in defining and achieving functional coverage metrics.
- Assertions: Practical experience with System Verilog Assertions (SVA) for design correctness.
- EDA Tools: Hands-on proficiency with industry-standard simulation tools (e.g., Synopsys VCS/Xcelium, Cadence Incisive/Xcelium, Mentor Questa Sim) and debugging tools.
- Scripting: Proficient in at least one scripting language (e.g., Python, Perl, Tcl) for automation of verification flows and data analysis.
- Linux/Unix Environment: Comfortable working in a Linux/Unix command-line environment.

- Problem-Solving & Debugging: Excellent analytical, problem-solving, and debugging skills with a meticulous attention to detail.
- Communication: Strong verbal and written communication skills to articulate complex technical concepts and collaborate effectively with cross-functional teams.

Qualifications:

- Education: Bachelor's or Master's degree in Electronics & Communication Engineering (ECE), Electrical Engineering (EE), Computer Science Engineering (CSE), or a related field.
- Experience: 0-1 year of relevant industry experience in VLSI Design Verification. (For exceptional freshers with strong project work/Master's, this could be an entry point as well).

Nice to Have:

- Experience with Python/TCL scripting for automation.
- Exposure to AMBA protocols (AXI, AHB, APB).
- Familiarity with Lint, CDC, STA concepts.
- Certification in VLSI design or verification courses.

Compensation:

Competitive and based on experience and engagement level.