

Job Title: VLSI Trainer (Jr)

Location: Hyderabad

Type: Part-time / Full-time / Contract

Experience Level: 0 - 3 Years (Preferred)

Job Summary:

We are looking for an experienced and passionate RTL Design and Verification Trainer to train and mentor students in Digital Design, Verilog/System Verilog, UVM, and industry-standard verification methodologies. You will play a key role in preparing learners for careers in the VLSI industry by delivering hands-on, application-oriented sessions.

Key Responsibilities:

- Deliver structured training in RTL design using Verilog/VHDL and System Verilog.
- Provide assignments, labs, and project evaluations.
- Mentor students on best practices in coding, simulation, synthesis, and debugging.
- Stay updated with latest trends in VLSI tools and methodologies (Vivado, Cadence, Synopsys, Mentor, etc).
- Optionally contribute to course content development and curriculum improvements.

Required Skills:

- Strong knowledge of Digital Design concepts.
- Hands-on experience with Verilog, System Verilog, UVM.
- Proficiency in simulation tools (Model Sim, VCS, Questa, etc.) and synthesis tools (Design Compiler, Genus, etc.).
- Experience in writing testbenches, assertions, and working with functional coverage.
- Familiarity with FPGA boards and lab setup (optional but a plus).
- Excellent communication and teaching/presentation skills.
- Ability to explain complex technical concepts in simple terms.

Qualifications:

- B.E/B.Tech or M.E/M.Tech in ECE/EEE or related fields.
- 0 - 3 years of experience in RTL design/verification or training roles.
- Prior teaching, mentoring, or corporate training experience is highly preferred.

Nice to Have:

- Experience with Python/TCL scripting for automation.
- Exposure to AMBA protocols (AXI, AHB, APB).
- Familiarity with Lint, CDC, STA concepts.
- Certification in VLSI design or verification courses.

Compensation:

Competitive and based on experience and engagement level.